



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/539,111

12/15/2005

Dieter E Staiger

DE920020033US1

9027

75949

7590

03/26/2010

IBM CORPORATION

C/O: VanCott Bagley, Cornwall & McCarthy

36 South State Street

Suite 1900

Salt Lake City, UT 84111

EXAMINER

RHU, KRIS M

ART UNIT

PAPER NUMBER

2184

MAIL DATE

DELIVERY MODE

03/26/2010

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/539,111	<b>Applicant(s)</b> STAIGER, DIETER E	
	<b>Examiner</b> KRIS RHU	<b>Art Unit</b> 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/3/09, 3/3/10</u> .   | 6) <input type="checkbox"/> Other: _____                          |

***DETAILED ACTION***

***Information Disclosure Statement***

1. The information disclosure statement filed 3/3/10 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because an English copy of the abstract of Japanese Publication 2002-542743 was not submitted. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Staiger (US 2004/0205386 A1), herein referred to as Staiger '386.

Referring to claim 1, Staiger '386 teaches a circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising: a) number of controller means (**Specific I/O Subsystems 26 and 34**) for controlling respective application specific ECUs (**ECUs 12 and 18, Figure 3**), each of the controller means comprising a number of application-specific support functions and I/O subsystems; and b) a number of processor units (**CPUs 20 and 28, Figure 3**) each having an I/O-interface operatively connecting to a respective one of the controller means and supplying that controller means with computing power, wherein at least one of the processor units and a respective controller means are implemented on different chips (**Note CPU 20 is in ECU 12 and Specific I/O Subsystem 26 is not, Figure 3**).

As to claim 2, Staiger '386 teaches the circuit according to claim 1, further comprising mapping means (**"A Dynamic Storage Subsystem Morphing (DSSM) mechanism is implemented connected to said plurality of resources, which reserves some storage area for each non-donor ECU, ready for any inventionally provided 'slot-down/slot-up' access by a respective non-donor ECU having a storage subsystem breakdown", Paragraph 0034, Lines 5-10**) for mapping the I/O subsystems to the processor units, and a General Controller Unit (**"In absence of an integrated ASIC architecture a fast FET-switch-based multiplexing mechanism is provided**

**for fast switching between both processors, such that the timing requirements of the processors are achieved”, Paragraph 0035, Lines 4-8)** operatively coupled to the mapping means and configured to dynamically switch at least one of the processor units into communication with a selected controller means based on processor timing requirements.

As to claim 3, Staiger '386 teaches the circuit according to claim 2, further comprising: a primary layer comprising basic configuration layout data and an interface means **(DSSM 40, Figure 3)** for connecting to the number of processor units; and a secondary layer comprising a preprogrammed, autonomic state switching means **(Autonomic System Controller 60, Figure 6)**, a preprogrammed emergency switching means **(“monitoring the operation of said ECUs, in case of breakdown of a non-donor ECU storage subsystem”, Paragraph 0043, Lines 1-2)**, and a port interface means **(Note Subsystem 26 is an I/O subsystem. Thus, it has a port interface to be able to perform the I/O)** connected to at least one of the I/O subsystems.

As to claim 4, Staiger '386 teaches the circuit according to claim 3, further comprising an additional controller operatively coupled to the General Controller Unit and configured to implement a monitoring function means **(“monitoring the operation of said ECUs, in case of breakdown of a non-donor ECU storage subsystem”, Paragraph 0043, Lines 1-2)** for monitoring the operational status of the processor units and the controller means.

As to claim 7, Staiger '386 teaches an embedded system (**“The present invention relates to the field of embedded processing systems and to autonomic embedded computing solutions”, Paragraph 0001, Lines 1-3**) having an electronic circuit according to claim 1.

Referring to claim 8, Staiger '386 teaches a method of operating an embedded processing system comprising: controlling a number of electronic control units (**ECUs 12 and 18, Figure 3**) with a number of interface expander controllers (**Specific I/O Subsystems 26 and 34**), wherein said interface expander controllers are disposed on a separate chip (**Note CPU 20 is in ECU 12 and Specific I/O Subsystem 26 is not, Figure 3**) from said electronic control units; and providing computing power to said interface expander controllers with a separate number of processors (**CPUs 20 and 28, Figure 3**).

As to claim 9, Staiger '386 teaches the method of claim 8, further comprising selectively providing communication between said interface expander controllers and said processors with a General Controller Unit (**“In absence of an integrated ASIC architecture a fast FET-switch-based multiplexing mechanism is provided for fast switching between both processors, such that the timing requirements of the processors are achieved”, Paragraph 0035, Lines 4-8**).

As to claim 10, Staiger '386 teaches the method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific Integrated Circuit (**“The present invention can be realized in**

**hardware, or a combination of hardware and software, for example in a programmable ASIC form or with selected units being implemented in any type of hardware implementation as required by the applicational use of the embedded system”, Paragraph 0100, Lines 1-5).**

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staiger '386.

As to claim 5, Staiger '386 does not appear to explicitly teach the circuit according to claim 1, further comprising a database storing instructions on how to handle specific errors associated with the number of processor units.

Staiger '386 does, however, teach “[performing] a checksum analysis, prior art error analysis and acting according to their results” (Paragraph 0054, Lines 10-11).

At the time of the invention, it would have been obvious to one of ordinary skill in the art having the teachings of Staiger '386 before him or her, to modify Staiger '386 to include a database storing instructions on how to handle specific

errors associated with the number of processor units since different errors may yield different results during checksum analysis. Having a database storing each type of error and their corresponding result during checksum would facilitate the determination of how to handle such errors.

Therefore, it would have been obvious to modify Staiger '386 to obtain the invention as specified in the instant claim.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staiger '386 in view of Phipps (US 6,579,231 B1), herein referred to as Phipps '231.

As to claim 6, Staiger '386 does not appear to teach the circuit according to claim 1, further comprising a number of emergency controllers for continuously storing global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case.

Phipps '231, however, teaches the circuit according to claim 1, further comprising a number of emergency controllers **(Unit 12, Figure 1)** for continuously storing **(PDU 14, Figure 1)** global positioning system (GPS) coordinates and configured to send an emergency signal **(“For example, if data from the monitoring device indicates heart fibrillation, emergency transmission sends a page in accordance with an emergency dialing sequence and transmits device ID, current GPS coordinates, and current data from the monitoring device”, Column 7 Lines 51-55)** including the



coordinates in case a number of external sensor devices detect an emergency case.

Staiger '386 and Phipps '231 are analogous art since Staiger '386 teaches ECUs that are dedicated to perform specific functions and Phipps '231 teaches a specific function.

At the time of the invention, it would have been obvious to one of ordinary skill in the art having the teachings of Staiger '386 and Phipps '231 before him or her, to modify Staiger '386 to include comprising a number of emergency controllers for continuously storing global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case, as taught by Phipps '231, since it merely involve replacing a specific function of one the ECUs taught in Staiger '386 with the function taught in Phipps '231. Though Staiger '386 teaches ECUs that perform specific functions for vehicles and the specific function taught in Phipps '231 is the monitoring of a human being's condition and the sending of an emergency signal when an emergency case (ex. heart attack, heart failure) is detected, it would be obvious to similarly monitor the condition of a vehicle and send an emergency signal when it detects an emergency case (ex. car failure, car crash).

Therefore, it would have been to combine Phipps '231 with Staiger '386 to obtain the invention as specified in the instant claim.

***Response to Arguments***

7. Applicant's arguments filed 12/3/09 have been fully considered but they are not persuasive.

8. Regarding the 35 U.S.C. §112 rejection, Applicant's argument is persuasive. The §112 rejection is withdrawn.

9. Regarding the 35 U.S.C. §102(b) rejection, Applicant argued, **"In light of the above facts, it is impossible for the Staiger reference to qualify as prior art under 35 U.S.C. § 102(b) against the present application. Particularly, § 102(b) requires that an allegedly anticipating reference be 'a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.'** (Emphasis added). **This condition cannot be met because the present application was filed more than three months prior to the Staiger reference, and the foreign priority date of the present application is "the date of application for patent in the United States" under § 102(b). 35 U.S.C. § 119(a); 37 C.F.R. § 1.55"**, in lines 6-13 of page 7.

Applicant's argument is not persuasive. "[No] patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before *the date of the actual filing of the application in this country*, or which had been in public use or on sale in this country more than one year prior to such filing". See 35 U.S.C. § 119 (a). "If the application claims foreign priority under 35 U.S.C. 119(a)-(d) or 365(a) or (b), the effective filing date is the filing date of the U.S. application, unless situation (A) or (B) as set forth above applies. *The*

*filing date of the foreign priority document is not the effective filing date*, although the filing date of the foreign priority document may be used to overcome certain references. See MPEP § 706.02(b) and § 2136.05.” See MPEP § 706.02. Therefore, Staiger '386 is a reference against the present application under 35 U.S.C. § 102(b).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KRIS RHU whose telephone number is 571-270-1728. The examiner can normally be reached on MTWThF 8:30-6 EST.

Art Unit: 2184

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KR

/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184